REMARKS/ARGUMENTS

Claims 1-20 were previously pending in the application. Claims 2 and 18 are canceled; claims 1, 3-17, and 19-20 are amended; and new claims 21-25 are added herein. Assuming the entry of this amendment, claims 1, 3-17, and 19-25 are now pending in the application. The Applicant hereby requests further examination and reconsideration of the application in view of the foregoing amendments and these remarks.

Specification and Drawings:

In paragraph 1 of the office action, the Examiner objected to the drawings for not showing every feature specified in the claims. More specifically, the Examiner stated that:

> [T]he limitation "the amplifier comprises two or more amplification stages" in claim 8 and "the multiplexer includes a phase-locked loop circuit configured to lock the phase of the clock signal to the trunk NRZ signal" in claim 12 must be shown or the feature(s) canceled from the claim(s). No new matter should be added.

In response, the Applicant submits herewith a Transmittal of Corrected Drawings amending original Figs. 2 and 3 and adding new Fig. 3B. Support for the amendment of Fig. 2 can be found, e.g., on page 3, lines 18-20, and original claim 12. Support for new Fig. 3B can be found, e.g., on page 4, line 32, through page 5, line 5. The specification has been amended to reflect the addition of Fig. 3B and designation of original Fig. 3 as Fig. 3A.

Claim Objections:

In paragraph 2, the Examiner objected to claims 2-16 and 18-20 because "the preamble 'the invention of claim ..' is not appropriate and should be changed to 'the apparatus according to claim..' or 'the method according to claim ..' to be consistent with the language of the apparatus/method claimed in the invention." In response, the Applicant amended the preambles of now pending claims 3-16 and 17-20 to correct the specified informality.

Claim Rejections:

In paragraph 3, the Examiner rejected claims 1-4, 7-9, 13, 14, 17, and 18 under 35 U.S.C. § 103(a) as being unpatentable over Givehchi in view of Adham. In paragraph 4, the Examiner rejected claim 5 under 35 U.S.C. § 103(a) as being unpatentable over Givehchi in view of Adham, and in further view of Murai. In paragraph 5, the Examiner rejected claims 10, 11, 15, 16, and 20 under 35 U.S.C. § 103(a) as being unpatentable over Givehchi in view of Adham, and in further view of admitted prior art (APA). In paragraph 6, the Examiner rejected claim 12 under 35 U.S.C. § 103(a) as being unpatentable over Givehchi in view of Adham, and in further view of Mizoguchi. In paragraph 7, the Examiner objected to claim 6 as being dependent upon a rejected base claim, but indicated that claim 6 would be allowable if rewritten in independent form.

For the following reasons, the Applicant submits that all pending claims are allowable over the cited references and teachings.

Claims 1, 3-17, and 19-23:

Claim 1 is amended to include limitations previously present in original claims 2 and 3. Claim 17 is similarly amended.

Amended claim 1 is directed to an apparatus for converting a non-return-to-zero (NRZ) data signal to a return-to-zero (RZ) data signal. The apparatus has an amplifier configured to generate an

amplified RZ data signal corresponding to the NRZ data signal based on (i) the NRZ data signal and (ii) a clock signal synchronized with the NRZ data signal. The amplifier is a differential amplifier configured to generate the amplified RZ data signal based on a comparison between a first signal corresponding to the NRZ data signal and a second signal corresponding to the clock signal, wherein the second signal is the clock signal offset by a DC offset value.

Givehchi discloses an optical apparatus for generating an RZ optical data stream. A representative embodiment of this apparatus is shown in Givehchi's Fig. 2. More specifically, the apparatus has Mach-Zehnder modulator **204** configured to receive drive signal **217** from driver **232**, where the drive signal is generated based on output signal **236** of generator **240**. Generator **240** includes AND-gate **241** configured to apply a logical AND function to the digital input clock and data signals, thereby generating signal **236**. An example of signal processing in generator **240** is shown in Givehchi's Fig. 3.

In the rejection of original claim 3, the Examiner stated that:

> Givehchi in paragraph 0019, lines 14-18 discloses the signal generated 240 and 232 in response to the clock and data signals includes a DC component for achieving linear operation. Therefore, the data and clock signals (first and second signals) must be offset by a DC offset value to achieve linear operation.

For the following reasons, the Applicant submits that, in the above statement, the Examiner mischaracterized the teachings of Givehchi and used them improperly to reject original claim 3.

Givehchi's paragraph 0019 reads as follows:

> [0019] Moreover, FIG. 3 shows an RZ electrical data stream generated by the electrical data generator 240 from the exemplary clock and data voltages and provided on the line 236. The RZ electrical data stream includes bit values 1, 0, 1, 0, 1, 1, 0, and 1 at the respective clock cycles 0 through 7 corresponding to the bit values of the above-mentioned NRZ electrical data stream. The driver amplifier 232 receives the RZ electrical data stream on the line 236 and generates a modulation signal suitable for modulating the RZ electrical data stream onto the laser light propagating through the optical modulator 204. In a preferred embodiment, the optical modulator 204 is operated in the approximate linear region of the transfer function of the optical modulator 204. *Accordingly, the modulation signal generated by the driver amplifier 232 and provided to the optical modulator 204 preferably includes a DC component suitable for achieving such approximate linear operation of the optical modulator 204.* [Emphasis added.]

Presumably, in his rejection of original claim 3, the Examiner relied on the italicized sentence in paragraph 0019. However, it is clear from the very text of paragraph 0019 that Givehchi refers to adding a DC component to the signal applied to modulator **204** (i.e., the amplified RZ signal) and <u>not</u> to the clock signal applied to AND-gate **241**. Furthermore, AND-gate **241** is designed to process binary signals (see, e.g., Givehchi's Fig. 3) and, as such, interprets a first predefined voltage as a binary high and a second predefined voltage as a binary low. A DC bias added to the digital clock signal would lead to a deviation from the predefined voltages and, as a result, to errors in the output of AND-gate **241**. Thus, adding a DC offset value to the clock signal in the apparatus of Givehchi would substantially destroy its functionality. The Applicant therefore submits that Givehchi cannot possibly teach or suggest the limitation of "the second signal is the clock signal offset by a DC offset value," as explicitly recited in claim 1.

Adham discloses circuits that can be used to implement data buffers, AND-gates, OR-gates, and multiplexers in current-mode logic (CML) circuits. The Examiner does not contend that Adham teaches or suggests any of the limitations of original claim 3. Indeed, since the circuits of Adham are designed for processing logic signals, the addition of a non-zero bias value to one or more of these logic signals would seriously impede the circuit's operation.

Murai discloses an optical signal generation circuit, in which an NRZ optical input signal is split into first and second copies by an optical coupler. The first and second copies are then presented to a clock extraction circuit and an electro-absorptive (EA) modulator, respectively. The extracted clock signal is applied as a drive signal to the EA modulator, which is configured to modulate the second copy to produce an optical RZ signal. The Applicant submits that Murai does not teach or even suggest at least the limitations of "the amplifier is a differential amplifier configured to generate the amplified RZ data signal based on a comparison between a first signal corresponding to the NRZ data signal and a second signal corresponding to the clock signal; and the second signal is the clock signal offset by a DC offset value," as explicitly recited in claim 1.

Mizoguchi discloses a multiplexer with a built-in PLL circuit (see, e.g., Mizoguchi's Fig. 3). The Applicant submits that Mizoguchi does not teach or even suggest any of the limitations of claim 1.

For all these reasons, the Applicant submits that claim 1 is allowable over the cited references. For similar reasons, the Applicant submits that claim 17 is also allowable over the cited references. Since claims 3-16 and 19-23 depend variously from claims 1 and 17, it is further submitted that those claims are also allowable over the cited references. The Applicant submits therefore that the rejections of claims under § 103 have been overcome.

Claim 4:

Claim 4, which depends from claim 1, further specifies that the width of pulses representing data in the amplified RZ data signal is controlled by the DC offset value.

In the rejection of claim 4, the Examiner relied on the above-reproduced paragraph 0019 of Givehchi. As already explained above, adding a DC offset value to the clock signal in the apparatus of Givehchi would destroy its ability to generate an amplified RZ data signal. It is therefore clear that Givehchi cannot possibly teach or even suggest that the width of pulses representing data in the amplified RZ data signal is controlled by the DC offset value, the Examiner's statement to the contrary notwithstanding. The Applicant therefore submits that the rejection of claim 4 is improper and should be withdrawn.

Claims 22-23:

Claim 23, which depends from claim 1, further specifies that the apparatus of claim 1 includes a circuit adapted to generate a sinusoidal signal, said sinusoidal signal being the clock signal synchronized with the NRZ data signal. Claim 22 recites an analogous limitation. Support for claims 22-23 can be found, e.g., in Applicant's Fig. 4.

The Applicant submits that the cited references, independently or in combination, do not teach or suggest a combination of features corresponding to claim 23. This fact provides additional reasons for the allowability of claim 23 over the cited references. The Applicant further submits that these additional reasons also apply to claim 22. Advantageously, using a sinusoidal clock signal instead of, e.g., a square-wave clock signal, provides a convenient way of regulating the width of pulses representing data in the amplified RZ data signal. For example, said width can be adjusted by a simple adjustment of the DC offset value applied to the clock signal (see, page 5, lines 16-26).

Claims 24-25:

New claim 24 is equivalent to original claim 6 rewritten in independent form. Since original claim 6 was indicated as allowable, the Applicant submits that claim 24 is allowable. The Applicant further submits that, for the same reasons that claim 24 is allowable, claim 25 is also allowable.

In view of the above amendments and remarks, the Applicant believes that the now pending claims are in condition for allowance. Therefore, the Applicant believes that the entire application is now in condition for allowance, and early and favorable action is respectfully solicited.

Respectfully submitted,

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Annotated Marked-up Drawings

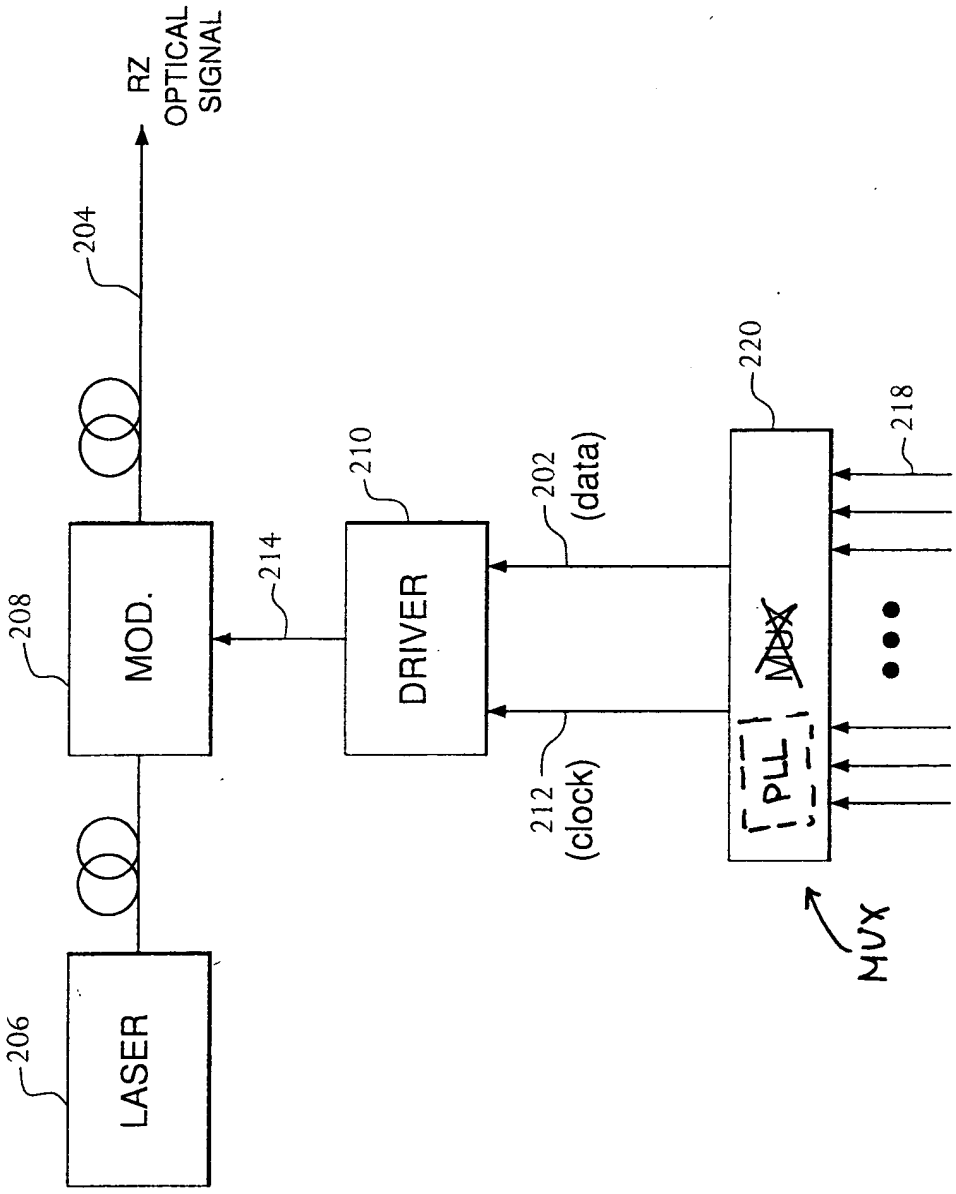
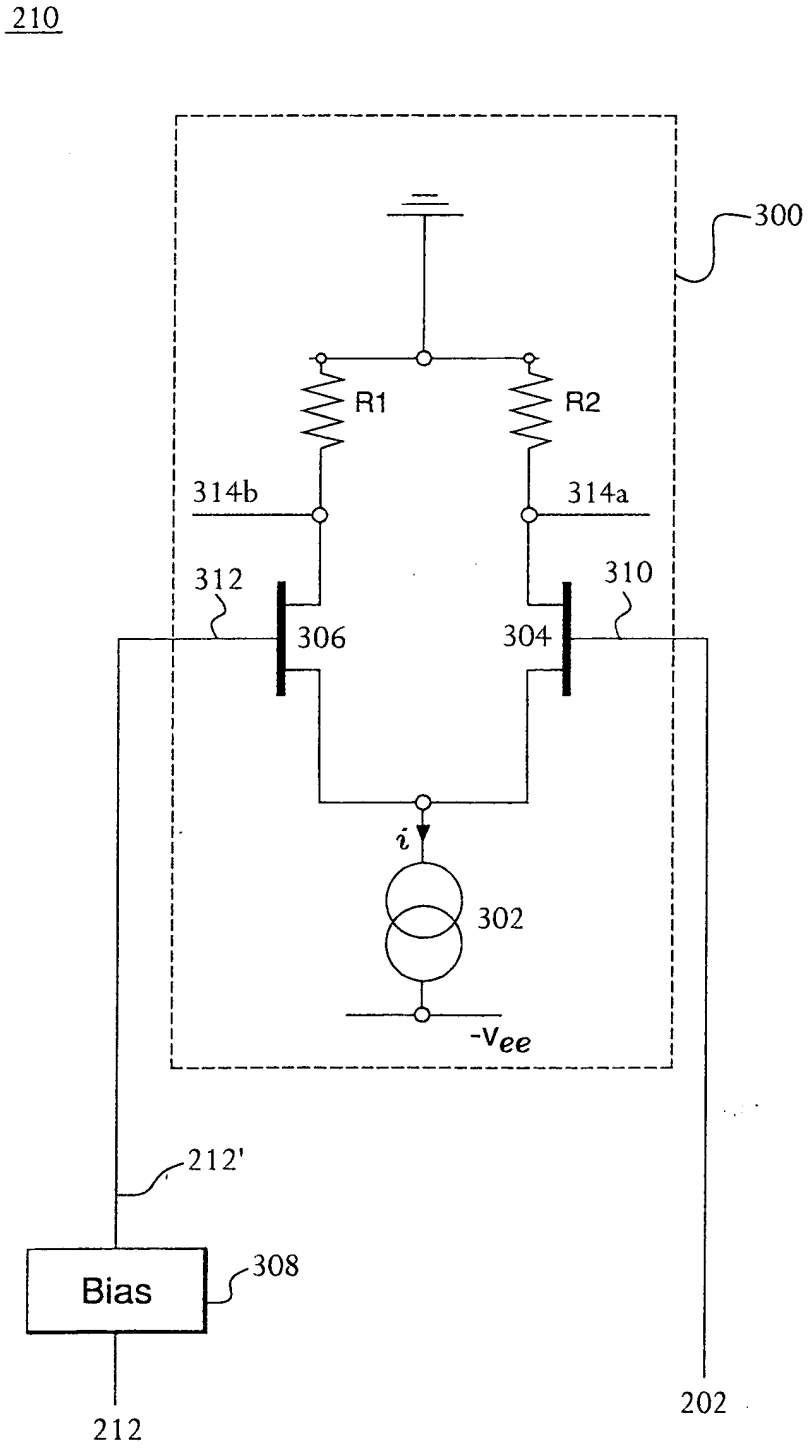


FIG. 2


210
300
R1
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314b
314a
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310
306
304
i
302
-Vee
212'
Bias
308
212
202

FIG. 3A